CSE 2441 CLASS AND LABORATORY SCHEDULE -- FALL 2015

8/24/2015 (draft)

(Schedule is subject to change at the instructor's discretion.)

Week	Weekly Reading	Class date	Tuesday (1) Lecture Topics	Class date	Thursday (2) Lecture Topics	Lab date	Lab topics	HW Due Dates
0	1.0-1.3.			8/27	Course overview, digital systems, number systems. Lab 0 preview.	8/28	Lab 0 -- Lab resources and procedures, DE1, BitBoard, basic logic gates. [BB]	
1	2.0-2.2, 1.4-1.6.	9/1	Combinational circuits; truth tables, functions, logic equations; basic gates -- AND, OR, NOT, NAND, NOR, XOR; basic adders. Lab 1 preview.	9/3	Signed-number representation, 2's complement number systems and arithmetic, digital codes.	9/4	Lab 1 -- Introduction to Quartus II.	HW#1 -- 9/3
2	2.3-2.4	9/8	Boolean algebra -- postulates and theorems. Functions and equations -- minterms, maxterms, SOP, POS, canonical forms. Lab 2 preview.	9/10	Minimization of logic equations and combinational circuits. Minimal forms.	9/11	Lab 2 -- Basic Adders. [BB]	HW#2 -- 9/10
3	2.4-2.5	9/15	Karnaugh maps. Incompletely specified functions. Lab 3 preview.	9/17	Combinational logic circuit analysis and design.	9/18	Lab 3 -- Two's-complement adder/subtractor. [BB]	HW#3 -- 9/17
4	3.0-3.2	9/22	Combinational logic circuit analysis and design (con't).	9/24	Catch up, design examples, and review.	9/25	Catch-up or get-ahead week.	HW#4 --9/24
5		9/29	**Examination 1.**	10/1	Timing diagrams and gate delay. Positive and negative logic. Lab 4 preview.	10/2	Lab4 -- DE1 programming and I/O. [DE1]	
6	3.3-3.5	10/6	Decoders , encoders, multiplexers and demultiplexers. Return exam. Lab 5 preview	10/8	Modular combinational logic with Verilog.	10/9	Lab 5 -- Four-function arithmetic/logic unit (ALU). [DE1]	
7	4.0-4.4	10/13	Sequential circuits and flip-flops.	10/15	Sequential circuits, flip flops, and registers.	10/16	Catch-up or get-ahead week.	HW#5 -- 10/13
8	4.5-4.6	10/20	Counters. Synchronous circuit analysis. Lab 6 preview.	10/22	Synchronous circuit design.	10/23	Lab 6 -- Intro to synchronous circuits. [BB]	HW#6 -- 10/20
9	5.0-5.2	10/27	Synchronous circuit design. Lab 7 preview.	10/29	Catch up, design examples, and review. Lab 8 preview.	10/30	Lab 7 -- Counters and displays. [DE1]	HW#7 -- 10/29
10		11/3	**Examination 2.**	11/5	Random Access Memory (RAM).	11/6	Lab 8 -- FSM design. [BB]	
11		11/10	Designing with Verilog. Return exam. Lab 9 preview.	11/12	Controllers and sequence recognizers.	11/13	Lab 9 -- TRISC controller lite. [DE1]	
12	5.3-5.4	11/17	Distribute and explain term design project assignment. Hierarchical design.	11/19	State reduction and state assignments.	11/20	Design project. [DE1]	HW#8 -- 11/17
13		11/24	Programmable logic. FPGAs. Cyclone II.	11/26	Thanksgiving Holiday.	11/27	Thanksgiving Holiday.	
14		12/1	Technical report writing.	12/3	Design examples.	12/4	Design project. [DE1]	
15		12/8	Review. **Design project demo deadline -- 6:00 PM.**	**12/9**	**Design project report due by 5:00 PM.**			
		12/15	**Final exam -- 2:00 to 4:30 PM**					