CSE 4323 CLASS SCHEDULE -- FALL 2015
8/25/2015 (draft)
(Schedule is subject to change at the instructor's discretion.)

Week	Weekly Reading	Class date	Tuesday (1) Lecture Topics	Class date	Thursday (2) Lecture Topics	HW Due Dates
0	Chapter 1 (1.1 to 1.6)			8/27	Course Overview. Design goals. Technology trends.	
1		9/1	Computer System Organization and Architecture.	9/3	Processor Architecture.	
2	Appendix A	9/8	Instruction Set Architecture.	9/10	Internal Memory Architecture.	
3		9/15	External Memory Architecture.	9/17	Input/Output Architecture.	
4		9/22	Catch Up and Review	9/24	**Examination 1.**	
5	Chapter 1 (1.7 to 1.13), Appendix B	9/29	Quantitative Design and Analysis.	10/1	Memory Hierarchy.	
6		10/6	Memory Hierarchy.	10/8	Memory Hierarchy Design	
7	Chapter 2	10/13	Memory Hierarchy Design	10/15	Pipelining.	
8	Appendix C	10/20	Pipelining.	10/22	Pipelining.	
9		10/27	Pipelining.	10/29	Catch Up and Review.	
10	Chapter 3	11/3	**Examination 2.**	11/5	Instruction-Level Parallelism.	
11	Chapter 4	11/10	Instruction-Level Parallelism.	11/12	Data-level Parallelism	
12	Chapter 5	11/17	Data-level Parallelism	11/19	Thread-Level Parallelism	
13		11/24	Thread-Level Parallelism	11/26	***Thanksgiving Holiday***	
14	Chapter 6	12/1	Warehouse scale parallelism	12/3	Warehouse scale parallelism	
15		12/8	Review			
		12/15	**Final exam -- 11:00 AM to 1:30 PM**			