CSE 2441 CLASS AND LABORATORY SCHEDULE -- SPRING 2016

1/2/2016 (draft)

(Schedule is subject to change at the instructor's discretion.)

Week	Weekly Reading	Class date	Tuesday (1) Lecture Topics	Class date	Thursday (2) Lecture Topics	Lab date	Lab topics	HW Due Dates
1	1.0-1.3, 2.0-2.2.	1/19	Course overview, digital systems, number systems. Lab 0 preview.	1/21	Combinational circuits; truth tables, functions, logic equations; basic gates -- AND, OR, NOT, NAND, NOR, XOR;	1/22	Lab 0 -- Lab resources and procedures, DE1, BitBoard, basic logic gates. [BB]	
2	1.4-1.6, 2.3-2.4.	1/26	Signed-number representation, 2's complement number systems and arithmetic, digital codes. Lab 1 preview.	1/28	Boolean algebra -- postulates and theorems. Functions and equations -- minterms, maxterms, SOP, POS, canonical forms.	1/29	Lab 1 -- Introduction to Quartus II.	HW#1 -- 1/28
3	2.4-2.5	2/2	Minimization of logic equations and combinational circuits. Minimal forms. Lab 2 preview.	2/4	Karnaugh maps. Incompletely specified functions.	2/5	Lab 2 -- Basic Adders. [BB]	HW#2 -- 2/4
4	3.0-3.2	2/9	Combinational logic circuit analysis and design. Lab 3 preview.	2/11	Combinational logic circuit analysis and design (con't).	2/12	Lab 3 -- Two's-complement adder/subtractor. [BB]	HW#3 -- 2/11
5		2/16	Timing diagrams and gate delay. Positive and negative logic. Lab 4 preview.	2/18	Catch up, design examples, and review.	2/19	Catch-up or get-ahead week.	HW#4 --2/18
6	3.3-3.5	2/23	**Examination 1.**	2/25	Decoders , encoders, multiplexers and demultiplexers. Lab 4 reminder.	2/26	Lab4 -- DE1 programming and I/O. [DE1]	
7	4.0-4.4	3/1	Designing combinational logic with Verilog. Lab 5 preview. Return exam 1.	3/3	Sequential circuits and flip-flops.	3/4	Lab 5 -- Four-function arithmetic/logic unit (ALU). [DE1]	HW#5 -- 3/3
8	4.5-4.6, 5.0-5.1	3/8	Registers and counters. Lab 6 preview.	3/10	Synchronous circuit analysis.	3/11	Lab 6 -- Intro to synchronous circuits. [BB]	HW#6 -- 3/10
SB		3/15	*Spring Break*	3/17	*Spring Break*	3/18	*Spring Break*	
9	5.2	3/22	Synchronous circuit design. Lab 7 preview.	3/24	Controllers and sequence recognizers.	3/25	Lab 7 -- Counters and displays. [DE1]	HW#7 -- 3/3124
10		3/29	Catch up, design examples, and review. Lab 8 preview.	3/31	**Examination 2.**	4/1	Lab 8 -- FSM design. [BB]	
11		4/5	Designing sequential logic with Verilog.	4/7	Random Access Memory (RAM). Return exam.	4/8	Catch-up or get-ahead week.	
12	5.3-5.4	4/12	Distribute and explain term design project assignment. Hierarchical design. Report writing. Lab 9 preview.	4/14	State reduction and state assignments.	4/15	Lab 9 -- TRISC controller lite. [DE1]	HW#8 -- 4/14
13		4/19	Programmable logic. FPGAs. Cyclone II.	4/21	Multipliers and dividers.	4/22	Design project. [DE1]	HW#9 -- 4/21
14		4/26	Timers and clocks	4/28	Design examples.	4/29	Design project. [DE1]	
15		5/3	Design examples.	5/5	Design examples and review.	5/6	**Design project demonstration due by 5:00 PM.**	
		5/10	**Final exam -- 11:00 AM to 1:30 PM**					