CSE 2441 CLASS AND LABORATORY SCHEDULE -- FALL 2016

8/25/2016

(Schedule is subject to change at the instructor's discretion.)

Week	Weekly Reading	Class date	Tuesday (1) Lecture Topics	Class date	Thursday (2) Lecture Topics	Lab date	Lab topics	HW Due Dates
0	1.0-1.3.			8/25	Course overview, digital systems, number systems. Lab 0 preview.	8/26	Lab 0 -- Lab resources and procedures, DE1, BitBoard, basic logic gates. [BB]	
1	2.0-2.2, 1.4-1.6.	8/30	Combinational circuits; truth tables, functions, logic equations; basic gates -- AND, OR, NOT, NAND, NOR, XOR, basic adders. Lab 1 preview.	9/1	Digital codes. Signed-number representation, two's complement number systems and arithmetic .	9/2	Lab 1 -- Introduction to Quartus II.	HW#1 -- 9/1
2	2.3-2.5	9/6	Boolean algebra -- postulates and theorems. Functions and equations -- minterms, maxterms, SOP, POS, canonical forms. Lab 2 preview.	9/8	Minimization of logic equations and combinational circuits. Minimal forms.	9/9	Lab 2 -- Basic Adders. Two's-complement adder/subtractor. [BB]	HW#2 -- 9/8
3	3.0-3.2	9/13	Karnaugh maps. Incompletely specified functions.	9/15	Combinational logic circuit design. Functional completeness.	9/16	Catch-up or get-ahead week.	HW#3 -- 9/15
4	3.4-3.5	9/20	Combinational logic circuit analysis. Timing diagrams. Lab 3 preview.	9/22	Designing combinational logic with Verilog. Lab 4 preview.	9/23	Lab 3 -- DE1 programming and I/O. [DE1]	
5		9/27	Catch up, design examples, and review.	9/29	**Examination 1.**	9/30	Lab 4 -- Seven-segment displays and decoders. [DE1]	HW#4 --9/27
6	3.3, 4.0-4.2	10/4	Decoders , encoders, multiplexers and demultiplexers. Lab 5 preview.	10/6	Sequential circuits and flip-flops. Return exam 1.	10/7	Lab 5 -- Four-function arithmetic/logic unit (ALU). [DE1]	
7	4.3-4.6	10/11	Registers and counters.	10/13	Design examples. Modeling registers and counters with Verilog.	10/14	Catch-up or get-ahead week.	HW#5 -- 10/13
8	5.0-5.2	10/18	Synchronous circuit analysis. Lab 6 preview.	10/20	Synchronous circuit design.	10/21	Lab 6 -- Flip-flops, registers, and counters. [BB]	HW#6 -- 10/20
9	5.3-5.4	10/25	Controllers and sequence recognizers. Equivalent states and state reduction. Lab 7 preview.	10/27	Designing sequential circuits with Verilog.	10/28	Lab 7 -- FSMs and controllers. [BB]	HW#7 -- 10/27
10		11/1	TRISC organization. Random Access Memory (RAM). Lab 8 preview.	11/3	Catch up, design examples, and review.	11/4	Lab 8 -- TRISC lite controller and RAM. [DE1]	HW#8 -- 11/3
11		11/8	**Examination 2.**	11/10	Distribute and explain term design project assignment. Hierarchical design. Technical report writing.	11/11	Design project. [DE1]	
12		11/15	Programmable logic. FPGAs. Cyclone II.	11/17	Multipliers.	11/18	Design project. [DE1]	
13		11/22	Dividers.	11/24	Thanksgiving Holiday.	11/25	Thanksgiving Holiday.	
14		11/29	Timers and clocks.	12/1	Design examples.	12/2	Design project. [DE1]	HW#9 -- 12/1
15		12/6	Review. **Design project demo deadline -- 6:00 PM.**	**12/7**	**Design project report deadline -- 6:00 PM.**			
		12/13	**Final exam -- 2:00 to 4:30 PM**					