CSE 4323 CLASS SCHEDULE -- FALL 2016

8/25/2016

(Schedule is subject to change at the instructor's discretion.)

Week	Weekly Reading	Class date	Tuesday (1) Lecture Topics	Class date	Thursday (2) Lecture Topics	HW Due Dates
0	Chapter 1 (1.1 to 1.7)			8/25	Course Overview. Design goals. Technology trends.	
1	Chapter 1 (1.8 to 1.13)	8/30	Quantitative Design and Analysis.	9/1	Computer organization and architecture. Processor architecture.	HW #1 -- 9/6
2	Appendix A	9/6	Instruction Set Architecture.	9/8	Instruction Set Architecture.	HW #2 -- 9/13
3	Appendix C	9/13	Pipelining.	9/15	Pipelining.	HW #3 -- 9/20
4	Appendix C	9/20	Internal Memory Architecture	9/22	Internal Memory Architecture	HW #4 --9/27
5	Class Notes	9/27	Catchup and Review	9/29	**Examination 1.**	
6	Class Notes	10/4	External Memory Architecture	10/6	I/O Architecture and Buses	HW #5 -- 10/11
7	Appendix B	10/11	Cache Memory	10/13	Cache Memory	HW #6 -- 10/20
8	Appendix B	10/18	Cache Memory Optimization	10/20	Virtual Memory	HW #7 -- 10/27
9	Chapter 2	10/25	Memory Hierarchy Design	10/27	Memory Hierarchy Design	
10	Chapter 3	11/1	**Examination 2.**	11/3	Instruction-Level Parallelism.	
11	Chapter 4	11/8	Instruction-Level Parallelism.	11/10	Data-level Parallelism	HW #8 -- 11/15
12	Chapter 5	11/15	Data-level Parallelism	11/17	Thread-Level Parallelism	HW #9 -- 11/22
13	Chapter 5	11/22	Thread-Level Parallelism	11/24	***Thanksgiving Holiday***	
14	Chapter 6	11/29	Warehouse scale parallelism	12/1	Warehouse scale parallelism	HW # 10 -- 12/6
15		12/6	Review			
		12/13	**Final exam -- 11:00 AM to 1:30 PM**			