CSE 4323 CLASS SCHEDULE -- SPRING 2017

1/4/2017 -- DRAFT

(Schedule is subject to change at the instructor's discretion.)

Week	Weekly Reading	Class date	Tuesday (1) Lecture Topics	Class date	Thursday (2) Lecture Topics	HW Due Dates
1	Chapter 1	1/17	Course Overview. Design goals. Technology trends.	1/19	Quantitative Design and Analysis.	HW #1 -- 1/24
2	Appendix A	1/24	Computer organization and architecture. Processor architectures.	1/26	MIPS Instruction Set Architecture and Programming.	HW #2 -- 1/31
3	Appendix B	1/31	Internal Memory Organization.	2/2	Memory Hierarchy and Caching.	HW #3 -- 2/7
4	Chapter 2	2/7	Cache Memory Optimization	2/9	Memory Hierarchy Design	HW #4 -- 2/14
5		2/14	Virtual Memory	2/16	**Examination 1. (Chs. 1 and 2, Apps. A and C.)**	
6	Appendix C	2/21	MIPS instruction processing	2/23	Pipelining. MIPS pipeline.	HW #5 -- 2/28
7	Chapter 3	2/28	Instruction-Level Parallelism.	3/2	Instruction-Level Parallelism.	HW #6 -- 3/7
8		3/7	Instruction-Level Parallelism.	3/9	Instruction-Level Parallelism.	HW #7 -- 3/23
SB		3/14	***Spring Break***	3/16	***Spring Break***	
9	Class Notes	3/21	I/O Architecture and Control.	3/23	External Memory Organization and Architecture.	
10		3/28	**Examination 2 (App C, Ch. 3).**	3/30	Data-level Parallelism	
11	Chapter 4	4/4	Data-level Parallelism	4/6	Data-level Parallelism	
12		4/11	Data-level Parallelism	4/13	Data-level Parallelism	HW #8 -- 11/15
13	Chapter 5	4/18	Thread-Level Parallelism	4/20	Thread-Level Parallelism	HW #9 -- 11/22
14	Chapter 6	4/25	Thread-Level Parallelism	4/27	Warehouse scale parallelism	
15		5/2	Warehouse scale parallelism	5/4	Review	HW # 10 -- 12/6
		5/9	**Final exam -- 11:00 AM to 1:30 PM**			