Course Syllabus

EE 2403
Spring, 2015
M,W,F 8:00 – 8:50 am
NH, Room 108

Instructor: Prof. Jonathan Bredow

Office: Room 522 Nedderman Hall

Office Hours: M,W,F 9:00-9:30am, otherwise by appointment.

Phone: 817-272-3934

Mailbox: Room 549 Nedderman Hall

Email: jbredow@uta.edu

Instructor WWW site: www.uta.edu/ee

Course WWW site: https://elearn.uta.edu/

Required Textbook(s): Microelectronic Circuits, A. Sedra and K. Smith, 6th ed., Oxford University Press, 2010.

Optional material: National Instruments NI myDAQ **(**for experimenting with circuits)

Reference Materials: See materials provided on Blackboard.

Course Description: Analysis and design of electronic circuits. Review of DC biasing, small-signal frequency response, differential and operational amplifier design and applications, IC terminal behaviors.

Course Learning Goals/Objectives: Refer to Table 1 at the end of the syllabus

ABET Outcomes coverage in the course: Refer to Table 2 at the end of the syllabus

Attendance Policy:

Drop Policy:

As per University guidelines. See the Registrar's Bulletin or the University Calendar for drop dates.

Tentative Lecture/Topic Schedule (Course Content) and Specific Course Requirements w/Descriptions:

Grade Computation:	Exam I, Exam II	each 20%
	Lab	25%*
	Homeworks, projects, quizzes	15%
	Final Exam	20%

*Note students must achieve passing score on the lab component to pass the class.

Policies: Late homeworks, projects and not showing for exams is inexcuseable with-out approval of instructor prior to due date or exam date.

(See lab schedule below)

Jan.	21	Introduction/Signals and Amplifiers (Chpt. 1)
"	23	" " " "
"	26	" " " "
"	28	" " " "
"	30	" " " "
Feb.	2	Operational Amplifiers (Chpt. 2)
"	4	" " " "
"	6	" " " "
"	9	" " " "
"	11	Semiconductors (Chpt. 3)
"	13	" " " "
"	16	" " " "
"	18	" " " "
"	20	" " " "
"	23	" " " "
"	25	" " " "
".	27	Exam I
Mar.	2	Diodes (Chpt. 4)
"	4	" " " "
"	6	" " " "
"	9	Spring Break
"	11	" " " "
"	13	" " " "
"	16	Diodes (Chpt. 4)
"	18	MOS Field-Effect Transistors (Chpt. 5)
"	20	" " " "
"	23	" " " "
"	25	" " " "
"	27	" " " "
"	30	" " " "
Apr.	1	Bipolar Junction Transistors (Chpt. 6)
"	3	" " " "
"	6	Exam II
"	8	Bipolar Junction Transistors (Chpt. 6)
"	10	" " " "
"	13	" " " "
"	15	Selected topics
"	17	" " " "
"	20	" " " "
"	22	" " " "
"	24	" " " "
"	27	" " " "
"	29	" " " "
May.	1	" " " "
"	4	Culmination
"	6	" " " "
"	8	" " " "

Final Exam: Friday May 15 8:00 - 10:30 am

Lab Schedule (tentative)

Week beginning with Monday	Topic
January 19	No Lab
January 26	Op amps

February 2	Op amps and terminal characteristics
February 9	IC Applications/projects
February 16	IC Applications/projects
February 23	Diodes and applications
March 2	Diodes and applications
March 9	Spring Break
March 16	MOSFETs and applications
March 23	MOSFETs and applications
March 30	BJTs and applications
April 6	Project work
April 13	Project work
April 20	Project work
April 27	Project work
May 4	TBD

If you require an accommodation based on disability, I would like to meet with you in the privacy of my office, during the first week of the semester, to make sure you are properly accommodated.

Student Evaluation of Teaching

Students will be asked to complete instructor/course evaluation forms at the end of the semester.

Americans with Disabilities Act:

The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 93112—The Rehabilitation Act of 1973 as amended. With the passage of new federal legislation entitled Americans with Disabilities Act – (ADA), pursuant to section 504 of The Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens.

As a faculty member, I am required by law to provide **"reasonable accommodation"** to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with **informing faculty at the beginning of the semester and in providing authorized documentation through designated administrative channels.**

Academic Dishonesty

It is the philosophy of The University of Texas at Arlington that academic dishonesty is a completely unacceptable mode of conduct and will not be tolerated in any form. All persons involved in academic dishonesty will be disciplined in accordance with University regulations and procedures. Discipline may include suspension or expulsion from the University.

"Scholastic dishonesty includes but is not limited to cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student or the attempt to commit such acts." (Regents' Rules and Regulations, Part One, Chapter VI, Section 3, Subsection 3.2, Subdivision 3.22).

ANY CHEATING WILL RESULT IN SEVERE PENALTIES.

Table 1: Statements of Course Objectives

Student is expected to demonstrate:	ABET Outcome mapping
Ability to design using op amps for a variety of applications.	a, c, k
Understanding of basic physics of semiconductor devices.	a, e
Ability to analyze and measure terminal electrical characteristics of small signal devices.	c, k
Ability to analyze and properly bias electronic circuits.	a, e, k
Understanding of low frequency small-signal circuit modeling and analysis.	c, e
Ability to design and construct simple and few-stage transistor amplifiers to achieve specifications on gain and input/output impedance.	c, k
Demonstrate ability to extend knowledge and skills gained in the course to somewhat more complex and varied circuits.	c, k
Working knowledge of Spice for linear transistor circuit analysis.	e, k
Clarity in written communication to explain approaches and results, and to compare with expected results.	g

Table 2: Coverage of ABET outcomes

ABET Outcome	Primary course component	Weight
(a) an ability to apply knowledge of mathematics, science, and engineering	**Exams, Homeworks, Projects**	**High**
(b) an ability to design and construct experiments, as well as to analyze and interpret data	**Lab**	**Moderate**
(c) an ability to design system, component, or process to meet desired needs	**Exams, Homeworks, Projects, Labs**	**High**
(d) an ability to function on multidisciplinary teams	**Lab**	**Low**
(e) an ability to identify, formulate, and solve engineering problems;	**Exams, Homeworks, Projects, Labs**	**High**
(f) an understanding of professional and ethical responsibility	**Not addressed**	**Not addressed**
(g) an ability to communicate effectively	**Projects, Labs**	**Moderate for written communication**
(h) the broad education necessary to understand the impact of engineering solutions in a global and societal context	**Not addressed**	**Not addressed**
(i) a recognition of the need for, and an ability to engage in lifelong learning	**Projects**	**Low**
(j) a knowledge of contemporary issues	**Not addressed**	**Not addressed**
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice	**Projects, Labs**	**High**
(l) an ability to apply probability and statistics, including applications appropriate to electrical engineering	**Exams, Homeworks**	**Low**