CSE 2441 CLASS AND LABORATORY SCHEDULE -- FALL 2018

8/15/2018

(Schedule is subject to change at the instructor's discretion.)

Week	*Weekly Reading*	*Class date*	*Tuesday (1) Lecture Topics*	*Class date*	*Thursday (2) Lecture Topics*	*Lab date*	*Lab topics*	*HW Due Dates*
0	0.0-0.7			8/23	Course overview, digital systems, basic gates: AND, OR, NOT, NAND, NOR, XOR, basic adders. Lab 0 preview.	8/24	Lab 0 -- Lab resources, policies and procedures, DE1, BitBoard, basic logic gates. [BB]	HW#1 -- 8/30
1	1.0-1.3, 2.0-2.2.	8/28	Combinational circuits; truth tables, functions, logic equations; number systems.	8/30	Signed-number representation, two's complement number systems and arithmetic . Digital codes. Lab 1 preview.	8/31	Lab 1 -- Introduction to Quartus II.	HW#2 -- 9/6
2	1.4-1.6, 2.3-2.4.	9/4	Boolean algebra -- postulates and theorems. Functions and equations -- minterms, maxterms, SOP, POS, canonical forms.	9/6	Minimization of logic equations and combinational circuits. Minimal forms. Lab 2 preview.	9/7	Lab 2 -- Basic Adders. Two's-complement adder/subtractor. [BB]	HW#3 -- 9/13
3	2.5.	9/11	Karnaugh maps. Incompletely specified functions.	9/13	Combinational logic circuit design and analysis. Timing diagrams.	9/14	Catch-up or get-ahead week.	HW#4 -- 9/20
4	3.0-3.2, 3.4-3.5.	9/18	Combinational logic circuit analysis. Propagation delay.	9/20	Catch up, design examples, and review. Lab 3 preview.	9/21	Lab 3 -- DE1 programming and I/O. [DE1]	
5		9/25	**Examination 1.**	9/27	Verilog modeling and programming. Lab 4 preview.	9/28	Lab 4 -- Seven-segment displays and decoders. [DE1]	HW#5 --10/4
6	3.3.	10/2	Higher-level combinational logic. Return exam 1.	10/4	Sequential circuits, flip-flops, registers, and counters. Lab 5 preview.	10/5	Lab 5 -- Four-function arithmetic/logic unit (ALU). [DE1]	HW#6 -- 10/11
7	4.0-4.6.	10/9	Verilog modeling of synchronous circuits. Circuit analysis.	10/11	Synchronous circuit design. Lab 6 preview.	10/12	Catch-up or get-ahead week.	HW#7 -- 10/18
8		10/16	Design examples -- controllers.	10/18	Sequence recognizers.	10/19	Lab 6 -- Flip-flops, registers, and counters. [BB]	HW#8 -- 10/25
9	5.4-5.5.	10/23	Synchronous circuit minimization. Equivalent states and state table reduction. State assignment.	10/25	Catch up, design examples, and review. Lab 7 preview.	10/26	Lab 7 -- FSMs and controllers. [BB]	
10		10/30	**Examination 2.**	11/1	TRISC organization. Random Access Memory (RAM). Lab 8 preview.	11/2	Lab 8 -- Random Access Memory (RAM). [DE1]	HW#9 -- 11/8
11		11/6	Announce term project assignment. Hierarchical design. Technical report writing.	11/8	Programmable logic. FPGAs. Cyclone II. Lab 9 preview.	11/9	Lab 9 -- TRISC lite controller. [DE1]	HW#10 -- 11/15
12		11/13	Multipliers.	11/15	Design examples.	11/16	Design project. [DE1]	
13	5.3.	11/20	Timers and clocks.	11/22	Thanksgiving Holiday	11/23	Thanksgiving Holiday	
14		11/27	Design examples.	11/29	Design examples.	11/30	**Project demo deadline -- 5:00 PM.**	
15		12/4	Review. **Project report deadline -- 11:59 PM.**	12/6	**Final exam -- 11:00 AM to 1:30 PM**			