CSE 2441 CLASS AND LABORATORY SCHEDULE -- SPRING 2019

1/11/2019 -- DRAFT

(Schedule is subject to change at the instructor's discretion.)

Week	*Weekly Reading*	*Class date*	*Tuesday (1) Lecture Topics*	*Class date*	*Thursday (2) Lecture Topics*	*Lab date*	*Lab topics*	*HW Due Dates*
1	0.0-0.7	1/15	Course overview, digital systems, basic gates: AND, OR, NOT, NAND, NOR, XOR, basic adders. Lab 0 preview.	1/17	Combinational circuits; truth tables, functions, logic equations; number systems.	1/18	Lab 0 -- Lab resources, policies and procedures, DE1, BitBoard, basic logic gates. [BB]	HW#1 -- 1/22
2	1.0-1.3, 2.0-2.2.	1/22	Signed-number representation, two's complement number systems and arithmetic . Digital codes. Lab 1 preview.	1/24	Boolean algebra -- postulates and theorems. Functions and equations -- minterms, maxterms, SOP, POS, canonical forms.	1/25	Lab 1 -- Introduction to Quartus II.	HW#2 -- 1/29
3	1.4-1.6, 2.3-2.4.	1/29	Minimization of logic equations and combinational circuits. Minimal forms. Lab 2 preview.	1/31	Karnaugh maps. Incompletely specified functions.	2/1	Lab 2 -- Basic Adders. Two's-complement adder/subtractor. [BB]	HW#3 -- 2/5
4	2.5.	2/5	Combinational logic circuit design and analysis. Timing diagrams.	2/7	Combinational logic circuit analysis. Propagation delay.	2/8	Catch-up or get-ahead week.	HW#4 -- 2/12
5	3.0-3.2, 3.4-3.5.	2/12	Multi-Level Circuits. Lab 3 preview.	2/14	Catch up, design examples, and review.	2/15	Lab 3 -- DE1 programming and I/O. [DE1]	
6		2/19	**Examination 1.**	2/21	Verilog modeling and programming. Lab 4 preview.	2/22	Lab 4 -- Seven-segment displays and decoders. [DE1]	HW#5 --2/28
7	3.3.	2/26	Higher-level combinational logic. Lab 5 preview. Return exam 1.	2/28	Sequential circuits, flip-flops, registers, and counters.	3/1	Lab 5 -- Four-function arithmetic/logic unit (ALU). [DE1]	HW#6 -- 3/7
8	4.0-4.6.	3/5	Verilog modeling of synchronous circuits. Circuit analysis.	3/7	Synchronous circuit design.	3/8	Catch-up or get-ahead week.	HW#7 -- 3/21
SB		***3/12***	***Spring Break***	***3/14***	***Spring Break***	***3/15***	***Spring Break***	
9	5.4-5.5.	3/19	Design examples -- controllers. Lab 6 preview.	3/21	Sequence recognizers. Lab 7 preview.	3/22	Lab 6 -- Flip-flops, registers, and counters. [BB]	HW#8 -- 3/28
10		3/26	Synchronous circuit minimization. Equivalent states and state table reduction. State assignment.	3/28	Catch up, design examples, and review. Lab 8 preview.	3/29	Lab 7 -- FSMs and controllers. [BB]	
11		4/2	**Examination 2.**	4/4	TRISC organization. Random Access Memory (RAM). Lab 9 preview.	4/5	Lab 8 -- Random Access Memory (RAM). [DE1]	
12		4/9	Announce term project assignment. Hierarchical design. Technical report writing.	4/11	Programmable logic. FPGAs. Cyclone II.	4/12	Lab 9 -- TRISC lite controller. [DE1]	HW#9 -- 4/16
13	5.3.	4/16	Multipliers.	4/18	Design examples.	4/19	Design project. [DE1]	HW#10 -- 4/25
14		4/23	Timers and clocks.	4/25	Design examples.	4/26	Design project. [DE1]	
15		4/30	Review.	5/2		5/3	**Project demo deadline -- 5:00 PM.** **Project report deadline -- 11:59 PM.**	
		5/7	**Final exam -- 11:00 AM to 1:30 PM**					