EE 2403-001
Electronics I

Summer 2018

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Catalog Course Description:

EE 2403 ELECTRONICS I. 4 Hours. Introduction to semiconductors, carrier statistics, drift and diffusion, semiconductor diodes, bipolar junction transistors (BJTs), and field-effect transistors (FETs). Circuit applications of diodes. Direct Current (DC) biasing and stability of circuits containing diodes, BJTs, and MOSFETs. Introduction to mid-band single stage small signal analysis of BJT and FET circuits. Laboratory experiments to complement concepts learned in class. Prerequisite: Grade C or better in both EE 2415 and MATH 2326.

Topics:

This course is an introduction into semiconductor devices and analog electronic circuits that uses these devices. Included in the first half of the course is the presentation of models for *pn*-junctions (diode), bipolar junction transistors (BJT), and MOS field-effect transistors (MOSFET). The development of methods and circuits for biasing these devices at desired dc operating points are given along with a treatment of bias sensitivity and stability. Topics are presented on the principles of small-signal linear amplifiers which include definitions of immittance and transfer functions, and the application of small-signal models in amplifier circuits. The second half of the course contains the design of single-stage amplifier circuits developed from various transistor configurations along with comparisons of characteristics.

Prerequisites:

EE 2415, MATH 2326.

Textbook:

1. A.S. Sedra and K.C. Smith, *Microelectronic Circuits, 6th Edition*, Oxford University Press, Inc., 198 Madison Ave., New York, NY 10016, 2010, ISBN 978-0-19-532303-0.
2. H.T. Russell, Jr., *Electronics Lab Manual, V2.0*, OPAL$_{tx}$, Fort Worth, TX, 2010.
3. Materials*xx* – a series of compressed (zipped) supplemental files made available on blackboard in timely intervals.

Tools:

1. Scientific calculator with matrix operations. Calculators such as the TI-89 Titanium, TI-Nspire™, CX CAS, HP-50G, and Casio FX-CP400-L are recommended. Calculators as components in communication devices are not allowed on exams.
2. PSPICE – found in the Cadence OrCAD 16.6 Lite Software package downloaded free from the Cadence Design Systems, Inc. website (www.cadence.com). Procedure for downloading the package is included in EE2403Materials1.
3. Toolbox (mandatory) – containing an assortment of electronics tools consisting of needle nose pliers, diagonal cutters, tweezers, precision knife set, pocket screwdrivers, and breadboard.
4. A good web browser.

Times and Location:

Lecture: **Section 001**, Monday and Wednesday, 8:00 am to 9:50 am, Nedderman Hall (NH), room 110.
Laboratory: **Section 101**, Monday and Wednesday, 10:30 am to 12:20 pm, Nedderman Hall (NH), room 148A.
Section 102, Monday and Wednesday, 10:30 am to 12:20 pm, Nedderman Hall (NH), room 148.

GTAs:
Lecture and lab: TBD.

EE 2403-001
Summer Lecture Schedule

Week/Date		Monday	Wednesday	Reading Assignment
1	6-4/6	Definition of semiconductors; carrier dynamics; semiconductor doping; donors and acceptors; intrinsic and extrinsic semiconductors; thermal equilibrium.	Resistivity and conductivity; resistance versus temperature; drift and diffusion; current densities; formation of the pn-junction diode; ideal diode theory; depletion region calculations.	Chap. 3 – 3.1 to 3.6
2	6-11/13	Neutral region derivations; diffusion characteristics; ideal IV-characteristics; saturation current.	The non-ideal diode; emission coefficient; bulk resistance; temperature effects; breakdown voltage; transient effects; diode models.	Chap. 4 – 4.1 to 4.5 Class notes
3	6-18/20	Diode model parameter extraction; example diode calculations and applications.	BJT fabrication and processing; fundamental theory of operation; the Ebers-Moll dc model.	Chap. 6 – 6.1 to 6.2.3
4	6-25/27	**Mid-Term Exam 1** Process-defined parameters; large-signal dc models for the internal and complete BJT.	Derivation of the BJT hybrid-pi small-signal BJT model; bias-dependent small-signal model components and parameters.	Chap. 6 – 6.5 to 6.6
5	7-2/4	Modifications to the hybrid-pi model; use of f_T and the Early voltage; example BJT calculations.	**July 4th Holiday**	Class notes and handouts Chap. 5 – 5.1 to 5.3
6	7-9/11	MOSFET device physics; basic theory of operation; the two-terminal MOS structure; depletion through inversion.	The four-terminal MOS structure; derivation of the channel current.	Chap. 5 – 5.5 to 5.6
7	7-16/18	**Mid-Term Exam 2** Large-signal and small-signal models; terminal capacitances; process-dependent model parameters; example MOSFET calculations.	BJT and CMOS dc bias circuits.	Chap. 6 – 6.7 to 6.8 Class notes and handouts
8	7-23/25	Bias sensitivity and stability; examples of dc bias circuits.	Small-signal amplifier principles; applications of small-signal models.	Chap. 1 – 1.1 to 1.6
9	7-30/8-1	Low frequency small-signal ac response characteristics of linear amplifiers.	Voltage and current gain, transimmittance functions; input and output immittance functions.	Chap. 1 – 1.6 to end Chap. 2 – 2.1 to 2.2 Class notes
10	8-6/8	High-frequency small-signal ac response characteristics of linear amplifiers; Bode plots.	Low-frequency inverting and non-inverting gain configurations; voltage gain, input and output impedance.	Chap. 2 – 2.2 to 2.4 Class notes and handouts
11	8-13	**Final Exam** **8:00 am to 10:00 am**		

References:

1. R.C. Dorf and J.A. Svoboda, *Introduction to Electric Circuits, 7th Edition*, John Wiley & Sons, Inc., 2006, ISBN-10 0-471-73042-2.
2. P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits, 4th Edition*, John Wiley & Sons, Inc., New York, NY, 2001.
3. S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits, 3nd Edition*, The McGraw-Hill Companies, Inc., New York, NY, 2001.
4. A.B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley and Sons, Inc., New York, NY, 1984.
5. M.S. Ghausi, *Principles of Linear Active Circuits*, McGraw-Hill Book Co., Inc., New York, NY, 1965.
6. J.M. Pettit and M.M. McWhorter, *Electronic Amplifier Circuits; Theory and Design*, McGraw-Hill Book Co., Inc., New York, NY, 1961.
7. P.E. Gray and C.L. Searle, *Electronic Principles; Physics, Models, and Circuits*, John Wiley and Sons, Inc., New York, NY, 1969.
8. P. Antognetti and G. Massobrio, *Semiconductor Device Modeling With SPICE, 2nd Edition*, McGraw-Hill Book Co., Inc., New York, NY, 1993.

Student Learning Outcomes:

EE 2403
Course Learning Objectives
and Assessment Approach

Number	Course Learning Objective (CLO)	ABET Outcome	Assessment Approach
1	An understanding of semiconductor basics and fundamentals.	a, e	exam problems
2	An understanding of the pn-junction diode theory of operation.	a, e	exam problems
3	An understanding of the BJT theory of operation.	a, e	exam problems
4	An understanding of the MOSFET and JFET theory of operation.	a, e	exam problems
5	An understanding of the derivation of large and small-signal models of semiconductor devices.	a, e	exam problems
6	An understanding of dc bias circuits and methods for semiconductor devices.	a, e	exam problems
7	An understanding of the importance of sensitivity functions in determining bias stability.	a, e	exam problems
8	An ability to apply circuit theory to analyze small-signal linear amplifiers.	a, e	exam problems
9	An understanding of small-signal response characteristics of linear amplifiers.	a, e	exam problems
10	An understanding of the design of op-amp inverting and non-inverting gain configurations.	a, e	exam problems

11	The application of computer tools and software in the solution of amplifier design problems.	a, k	labs
12	A working understanding of important analytical principles.	a, b, c	labs

Outcomes a-k
(a-k as listed by ABET)

a. an ability to apply knowledge of mathematics, science, and engineering;
b. an ability to design and construct experiments, as well as to analyze and interpret data;
c. an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability;
d. an ability to function on multidisciplinary teams;
e. an ability to identify, formulate, and solve engineering problems;
f. an understanding of professional and ethical responsibility;
g. an ability to communicate effectively;
h. the broad education necessary to understand the impact of engineering solutions in a global and societal context;
i. a recognition of the need for, and an ability to engage in lifelong learning;
j. a knowledge of contemporary issues;
k. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

General Lecture Section Information:

1. There are 21 class meetings scheduled for the 11 weeks of the Summer 2018 Semester. Nineteen of these meetings are devoted to in-class lectures, one scheduled for the July 4th holiday, and one devoted to the Final Examination.
2. Your 100% attendance in lectures and labs is mandatory and required. This requirement will not be waived for any reason.
3. There will be five to six homework assignments, usually given on one and one-half week intervals. Each assignment requires about five to ten hours for completion. These assignments will be graded and will be included as part of your total course grade. Experience has shown that students who spend the necessary time to work these assignments usually do quite well on the examinations. Solutions to homework problems will be posted on blackboard by the end of the day the assignment is due. Homework turned in after the solutions have been posted will not be counted and will receive a grade of zero.
4. Mid-term examinations will be given on the 4th and 7th weeks and will be one hour written exercises.
5. The final examination will be given on **Monday, August 13, 2018 from 8:00 am to 10:00 am in NH110** and will be a comprehensive written examination. **NOTICE**: The UTA registrar has demanded a firm, unforgivable final date (four calendar days after the last final examination date) for the submission of course grades from all instructors. Because of this rigid schedule, the date planned for the final examination (**Monday, August 13, 2018 from 8:00 am to 10:00 am in NH110**) is fixed and will not be changed for any reason. Therefore, all students, without exception, **must** take the final examination at this time.
6. You are respectively requested to turn off all communication devices while in the Lecture/Lab Sections. Communication devices of any type are not allowed to be used on all exams. No exceptions. Calculators without communication capability are permitted.
7. All examinations will be pencil, paper, and calculator exercises. All students will take these exams at the scheduled times in the classroom.
8. There will be **no** late or make-up mid-term examinations given unless a written request has been submitted to and approved by the instructor at least two weeks prior to the examination date. As a rule, make-up examinations are several orders of magnitude more difficult than examinations given on the scheduled dates. Please be advised that illness or any other absence on the examination date does not constitute a valid reason for a make-up examination.
9. **IMPORTANT NOTICE**: Failure to take (either scheduled or approved make-up) any or all exams (mid-terms and final) will automatically result in a letter grade of 'F' for the course. You are required to take all exams.

10. The *total grade* (T) for this course is based upon the grades for homework, labs, two mid-term exams, and the final exam. The total T is computed from

$$T = 0.1 \cdot (HW + LA) + 0.25 \cdot (MTE1 + MTE2) + 0.3 \cdot FE \quad (1)$$

HW = homework average
LA = lab grade
MTE1 = mid-term exam 1 grade
MTE2 = mid-term exam 2 grade
FE = final exam grade

The letter grade is based on the range of the total grade shown below.

Percentage for Grades	
Total grade (T) range	Letter grade
88% - 100%	A
75% - 87%	B
63% - 74%	C
50% - 62%	D
0% - 49%	F

11. Office hours are posted outside my office (NH526). If you have any questions and/or adverse difficulty with the lectures or class material, I strongly suggest that you call or e-mail me (during regular working hours, of course). If necessary, a scheduled office visit can be arranged.
12. Additional important dates:
    First day of classes: - **Monday, June 4, 2018**.
    Census date – **Monday, June 4, 2018**.
    Last day to drop classes – **Thursday, July 5, 2018**.
    Last day of classes – **Thursday, August 9, 2018**.
    Final Exam date – **Monday, August 13, 2018**.

Drop Policy:

Please refer to the University policy for dropping courses.

Americans With Disabilities Act:

The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 92-112 - The Rehabilitation Act of 1973 as amended. With the passage of federal legislation entitled *Americans with Disabilities Act (ADA),* pursuant to section 504 of the Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens. As a faculty member, I am required by law to provide "reasonable accommodations" to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with informing faculty of their need for accommodation and in providing authorized documentation through designated administrative channels. Information regarding specific diagnostic criteria and policies for obtaining academic accommodations can be found at www.uta.edu/disability. Also, you may visit the Office for Students with Disabilities in room 102 of University Hall or call them at (817) 272-3364.

Student Support Services Available:

The University of Texas at Arlington supports a variety of student success programs to help you connect with the University and achieve academic success. These programs include learning assistance, developmental education, advising and mentoring, admission and transition, and federally funded programs. Students requiring assistance academically, personally, or socially should contact the Office of Student Success Programs at 817-272-6107 for more information and appropriate referrals.

Final Review Week:

A period of five class days prior to the first day of final examinations in the long sessions shall be designated as Final Review Week. The purpose of this week is to allow students sufficient time to prepare for final examinations. During this week, there shall be no scheduled activities such as required field trips or performances; and no instructor shall assign any themes, research problems or exercises of similar scope that have a completion date during or following this week unless specified in the class syllabi. During Final Review Week, an instructor shall not give any examinations constituting 10% or more of the final grade, except makeup tests and laboratory examinations. In addition, no instructor shall give any portion of the final examination during Final Review Week. Classes are held as scheduled during this week and lectures and presentations may be given.

E-Culture Policy:

The University of Texas at Arlington has adopted the University email address as an official means of communication with students. Through the use of email, UT-Arlington is able to provide students with relevant and timely information, designed to facilitate student success. In particular, important information concerning registration, financial aid, payment of bills, and graduation may be sent to students through email. All students are assigned an email account and information about activating and using it is available at www.uta.edu/email. New students (first semester at UTA) are able to activate their email account 24 hours after registering for courses. There is no additional charge to students for using this account, and it remains active as long as a student is enrolled at UT-Arlington. Students are responsible for checking their email regularly.

Ethics:

Student Responsibility

Undergraduate and graduate students assume full responsibility for knowledge of all University rules, regulations and deadlines published in the Undergraduate and Graduate Catalogs and of all departmental and program requirements concerning their degree programs.

Academic Dishonesty

All students are expected to pursue their academic careers with honesty and integrity. Academic dishonesty includes, but is not limited to, cheating on a test or other coursework, plagiarism (offering the work of another as one's own) and unauthorized collaboration with another person. Students found responsible for dishonesty in their academic pursuits are subject to penalties that may range from disciplinary probation, suspension or expulsion from the University. In accordance with the Rules and Regulations of the Board of Regents of The University of Texas System (Part One, Chapter VI), institutional procedures regarding allegations of academic dishonesty are outlined in Part Two, Chapter 2, of the U.T. Arlington Handbook of Operating Procedures. This information may be obtained by accessing the Dean of Students' Web site at www.uta.edu/studentaffairs/dos or the Student Judicial Affairs' Web site at www.uta.edu/studentaffairs/judicial affairs. Copies of each regulation can be obtained in the Dean of Students' Office on the lower level of the University Center.

Definitions (UTA Handbook of Operating Procedures)

F. scholastic dishonesty, including, but not limited to, cheating on an examination or an assignment, plagiarism, and collusion;

1. *cheating on an examination or an assignment* includes:
   a. copying the work of another, engaging in written, oral or any other means of communication with another, or giving aid to or seeking aid from another when not permitted by the instructor;
   b. using material during an examination or when completing an assignment that is not authorized by the person giving the examination or making the work assignment;
   c. taking or attempting to take an examination for another, or allowing another to take or attempt to take an examination for a student;
   d. using, obtaining, or attempting to obtain by any means, the whole or any part of an un-administered examination or work assignment;
   e. any act designed to give unfair advantage to a student or the attempt to commit such an act;
2. *plagiarism* means the unacknowledged incorporation of the work of another in work that is offered for credit;
3. *collusion* means the unauthorized collaboration with another in preparing work that is offered for credit.

The following is an excerpt from the College of Engineering's statement on Ethics, Professionalism, and Conduct of Engineering Students. Read the statement carefully, sign it, and return it to your instructor. You may make a copy for your records. Additional copies of this statement can be obtained from your instructor or the Office of the Dean of Engineering.

STATEMENT ON ETHICS, PROFESSIONALISM, AND CONDUCT FOR ENGINEERING STUDENTS

COLLEGE OF ENGINEERING
THE UNIVERSITY OF TEXAS AT ARLINGTON

The College cannot and will not tolerate any form of academic dishonesty by its students. This includes, but is not limited to cheating on examination, plagiarism, or collusion.

Cheating on an examination includes:

1. Copying from another's paper, any means of communication with another during examination, giving aid to or receiving aid from another during examination;
2. Using any material during examination that is unauthorized by the proctor;
3. Taking or attempting to take an examination for another student or allowing another student to take or attempt to take an examination for oneself.
4. Using, obtaining, or attempting to obtain by any means the whole or any part of an un-administered examination.

Plagiarism is the unacknowledged incorporation of another's work into work which the student offers for credit.
Collusion is the unauthorized collaboration of another in preparing work that a student offers for credit.

I have read and I understand the above statement.

In addition, I understand that, in order to ensure fairness to all students, exams will be proctored and possibly video recorded.

Course and section number: ____EE 2403-001/101/102_____

Date: _____

Student's signature: _____

Student's name, printed: _____

Student's ID number: _____

Student's e-mail address: _____
(please print clearly)