# EE 3444-001
# Electronics II

Spring 2017
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### Catalog Course Description:
**EE 3444 ELECTRONICS II** (3-3) Low and high frequency characteristics and circuit models for diodes, bipolar junction transistors (BJTs), and field effect transistors (FETs). Analysis and design of full spectrum small signal BJT and FET circuits. Analysis and transistor level design of active filters, oscillators, feedback configurations, and multistage differential and operational amplifiers. Concurrent laboratory exercises in support of the topics covered in class. Prerequisite: Grade C or better in both EE 2403 and EE 3446.

### Topics:
EE 3444 covers the analysis and design of analog bipolar junction transistor (BJT) and field-effect transistor (JFET and CMOS) amplifier circuits. The first part of the course includes a review of the small-signal models of bipolar devices (diodes, BJT's, and FET's), current sources and current mirrors, single-stage bipolar dc biasing methods, bias sensitivity and stability concepts, principles of small-signal ac amplifiers, a review of immittance and transfer functions, the use of small-signal BJT models in amplifier circuits, the frequency response characteristics of single-stage amplifiers, and the Miller effect and model. The second half of the course is concerned with multiple-stage cascade amplifier designs, cascode amplifier designs, differential amplifier analysis and design, and circuits used in operational amplifiers which include the dc bias and interstage coupling circuits as well as output stage designs. Additional topics include the analysis of feedback amplifiers, oscillators, and single and multiple amplifier biquad filters.

### Prerequisites:
EE 2403, EE 3446

### Textbook & Supplements:
1. A.S. Sedra and K.C. Smith, *Microelectronic Circuits, 6th Edition*, Oxford University Press, Inc., 198 Madison Ave., New York, NY 10016, 2010, ISBN 978-0-19-532303-0.
2. H.T. Russell, Jr., *Electronics Lab Manual, V2.0*, OPAL$_{tx}$, Fort Worth, TX, 2010.
3. Materials*xx* – a series of compressed (zipped) supplemental files made available on blackboard in timely intervals.

### Tools:
1. Scientific calculator with matrix operations. Calculators such as the TI-89 Titanium, TI-Nspire™, CX CAS, HP-50G, and Casio FX-CP400-L are recommended. Calculators as components in communication devices are not allowed on exams.
2. PSPICE – found in the Cadence OrCAD 16.6 Lite Software package downloaded free from the Cadence Design Systems, Inc. website (www.cadence.com). Procedure for downloading the package is included in EE3444Materials1.
3. Toolbox (mandatory) – containing an assortment of electronics tools consisting of needle nose pliers, diagonal cutters, tweezers, precision knife set, pocket screwdrivers, and breadboard.
4. A good web browser.

### Times and Location:
*Lecture Section 001* – Tuesday and Thursday, 8:00 am to 9:20 am, WH311.
*Lab Section 101* – Wednesday, 11:00 am to 1:50 pm, NH148.
*Lab Section 102* – Friday, 11:00 am to 1:50 pm, NH148.

**GTAs:**
*Lecture* – TBD.
*Lab* – TBD.

| Spring 2017 EE 3444-001<br>Lecture Schedule | | | | |
|---|---|---|---|---|
| **Week/Date** | | **Tuesday** | **Thursday** | **Reading Assignment** |
| 1 | 1-17/19 | dc bias circuits for single stage BJT amplifiers; voltage divider and self-bias networks. | dc bias circuits for single stage MOS amplifiers; voltage divider and self-bias networks. | Chapt. 6 – all.<br>Chapt. 7 – 7.1 to 7.3.<br>Materials1, Materials2. |
| 2 | 1-24/26 | Small-signal amplifier principles; frequency ranges. | Low and mid-band frequency range response functions. | Chapt. 7 – 7.3 to 7.4.<br>Materials3. |
| 3 | 1-31/2-2 | Single-stage BJT amplifier configurations; CE, CB, CC. | Single-stage MOS amplifier configurations; CS, CG, CD. | Chapt. 7 – 7.5 to end.<br>Materials4. |
| 4 | 2-7/9 | The Miller effect and Miller model; dominant pole theory. | Derivation of the BJT Miller model and the unilateral (U) model. | Chapt. 10 – 10.1 to 10.4.<br>Materials4. |
| 5 | 2-14/16 | Maximization of the GBW. | Derivation of the MOS Miller model and the unilateral (U) model. | Chapt. 10 – 10.5 to 10.7. |
| 6 | 2-21/23 | Active current sources; current source parameters and models. | **Mid-Term Exam 1** | Chapt. 8 – 8.1 to 8.3.<br>Materials5. |
| 7 | 2-28/3-2 | Current source designs; self-bias and biased topologies. | JFET, BJT, and MOS current sources. | Materials5. |
| 8 | 3-7/9 | Current mirrors; current mirror parameters, the BJT Widlar current mirror. | The MOS Widlar current mirror. | Chapt. 8.4 to 8.6.<br>Materials5. |
| 9 | 3-14/16 | **Spring Break** | **Spring Break** | |
| 10 | 3-21/23 | Widlar current mirrors with emitter and source resistors. | Buffered, cascode, and the Wilson current mirrors. | Chapt. 8 – 8.6 to end.<br>Materials5. |
| 11 | 3-28/30 | Voltage differential amplifiers (VDA); current differential amplifiers (CDA). | Op-amp topology and stages; op-amp parameters. | Chapt. 9 – 9.1 to end.<br>Chapt. 13 – 13.1 to 13.2. |
| 12 | 4-4/6 | Op-amp circuits; loop-gain, stability, slew rate. | **Mid-Term Exam 2** | Chapt. 13 – 13.3 to end.<br>Materials6. |
| 13 | 4-11/13 | Feedback amplifiers topologies; comparing and sampling. | Feedback amplifier analysis – a two-port approach. | Chapt. 11 – 11.1 to 11.4.<br>Materials7. |
| 14 | 4-18/20 | Open and closed loop parameters. | Amplifier parameters affected by feedback. | Chapt. 11 – 11.5 to end.<br>Materials7. |

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|---|---|---|---|---|
| 15 | 4-25/27 | Linear continuous-time active RC filters. | Biquadratic (2nd order) response functions. | Chapt. 17 – 17.1 to 17.5. Materials8. |
| 16 | 5-2/4 | Single amplifier biquad (SAB) filters. | Multiple amplifier biquad (MAB) filters. | Chapt. 17 – 17.7 to 17.8. Materials8. |
| 17 | 5-9/11 | **Final Exam<br>Tuesday, May 9, 2017<br>8:00 am to 10:30 am** | | |

**References:**


1. P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits, Fourth Edition*, John Wiley & Sons, Inc., New York, NY, 2001.
2. S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits, 3nd Ed.*, The McGraw-Hill Companies, Inc., New York, NY, 2001.
3. A.B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley and Sons, Inc., New York, NY, 1984.
4. M.S. Ghausi, *Principles of Linear Active Circuits*, McGraw-Hill Book Co., Inc., New York, NY, 1965.
5. J.M. Pettit and M.M. McWhorter, *Electronic Amplifier Circuits; Theory and Design*, McGraw-Hill Book Co., Inc., New York, NY, 1961.
6. P.E. Gray and C.L. Searle, *Electronic Principles; Physics, Models, and Circuits*, John Wiley and Sons, Inc., New York, NY, 1969.
7. P. Antognetti and G. Massobrio, *Semiconductor Device Modeling With SPICE, Second Edition*, McGraw-Hill Book Co., Inc., New York, NY, 1993.
8. *SPICE 2 User's Guide*, University of California Berkeley, Electronics Research Labs, Berkeley, CA.


**Student Learning Outcomes:**

**EE 3444**
Course Learning Objectives
and Assessment Approach

| Number | Course Learning Objective (CLO) | ABET Outcome | Assessment Approach |
|---|---|---|---|
| 1 | Ability to develop small signal models for semiconductor devices (diode, BJT, JFET, and CMOS). | a, e | exam problems |
| 2 | Ability to analyze and design voltage and current-source biasing circuits for transistor amplifiers. | a, e | exam problems |
| 3 | Ability to analyze and design current mirrors. | a, e | exam problems |
| 4 | Ability to analyze small signal mid-band and high-frequency characteristics of transistor amplifier circuits. | a, e | exam problems |
| 5 | Ability to analyze and design single and multi-stage transistor amplifiers. | a, c, e | exam problems |
| 6 | Ability to analyze and design class AB output stages; how class AB bias and operation differs from that of class A. | a, e | exam problems |
| 7 | Ability to differentiate and analyze four basic feedback configurations for transistor circuits, including stability considerations. | a, e | exam problems |
| 8 | Working knowledge of PSPICE for verification of circuit performance. | a, e | lab experiments |

| | | | |
|---|---|---|---|
| 9 | Proper measurement techniques for characterizing semiconductor devices (diode, BJT, JFET, CMOS). | a, k | lab experiments |
| 10 | Proper measurement techniques for characterizing current sources, current mirrors, single-stage amplifiers, and multistage amplifiers. | a, e, k | lab experiments |
| 11 | Ability to analyze and design active circuits employing op-amps. | a, b, c | lab experiments |
| 12 | An ability to work as a member of a team. | d | lab experiments |
| 13 | An ability to understand and resolve professional ethical issues. | f | lab experiments |

Outcomes a-k
(a-k as listed by ABET)

a. an ability to apply knowledge of mathematics, science, and engineering;
b. an ability to design and construct experiments, as well as to analyze and interpret data;
c. an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability;
d. an ability to function on multidisciplinary teams;
e. an ability to identify, formulate, and solve engineering problems;
f. an understanding of professional and ethical responsibility;
g. an ability to communicate effectively;
h. the broad education necessary to understand the impact of engineering solutions in a global and societal context;
i. a recognition of the need for, and an ability to engage in lifelong learning;
j. a knowledge of contemporary issues;
k. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

### General Class Information:

1. There are 32 class meetings scheduled for the 17 weeks of the Spring 2017 Semester. Twenty-nine of these meetings are devoted to in-class lectures, three devoted to examinations – two mid-terms and one final.
2. Your 100% attendance in lectures and labs is mandatory and required. This requirement will not be waived for any reason.
3. There will be five to six homework assignments, usually given on two-week intervals. Each assignment requires about five to ten hours for completion. These assignments will be graded and will be included as part of your total course grade. Experience has shown that students who spend the necessary time to work these assignments usually do quite well on the examinations. Solutions to homework problems will be e-mailed to all students by the end of the day the assignment is due. Homework turned in after the solutions have been sent out will not be counted and will receive a grade of zero.
4. Mid-term examinations will be given on the $6^{th}$ and $12^{th}$ weeks, and will be 1.5 hour written exercises.
5. The final examination will be given on **Tuesday, May 9, 2017** and will be a comprehensive written examination. **NOTICE**: The UTA registrar has demanded a firm, unforgivable final date (four calendar days after the last final examination date) for the submission of course grades from all instructors. Because of this rigid schedule, the date planned for the final examination (**Tuesday, May 9, 2017, 8:00 am to 10:30 am**) is fixed and will not be changed for any reason. Therefore, all students, without exception, **must** take the final examination at this time.
6. You are respectively requested to turn off all communication devices while in the Lecture/Lab Sections. Communication devices of any type are not allowed to be used on all exams. No exceptions. Calculators without communication capability are permitted.
7. All examinations will be pencil, paper, and calculator exercises. All students will take these exams at the scheduled times in the classroom.
8. There will be no late or make-up mid-term examinations given unless a written request has been submitted to and approved by the instructor at least two weeks prior to the examination date. As a rule, make-up examinations are several orders of magnitude more difficult than examinations given on the scheduled dates. Please be

advised that illness or any other absence on the examination date does not constitute a valid reason for a make-up examination.

9. **NOTICE**: Failure to take (either scheduled or approved make-up) any or all exams (mid-terms and final) will automatically result in a letter grade of 'F' for the course. You are required to take all exams.
10. The *total grade* (T) for this course is based upon homework, recitation, two mid-term exams, and final exam grades. The total T is computed from

$$T = 0.1 \cdot (HW + RA) + 0.25 \cdot (MTE1 + MTE2) + 0.3 \cdot FE \quad (1)$$

HW = homework average
RA = recitation grade
MTE1 = mid-term exam 1 grade
MTE2 = mid-term exam 2 grade
FE = final exam grade

The letter grade is based on the range of the total grade shown below.

| **Percentage for Grades** | |
|---|---|
| Total grade (T) range | Letter grade |
| 88% - 100% | A |
| 75% - 87% | B |
| 63% - 74% | C |
| 50% - 62% | D |
| 0% - 49% | F |

11. Office hours are posted outside my office (NH526). If you have any questions and/or adverse difficulty with the lectures or class material, I strongly suggest that you call or e-mail me (during regular working hours, of course). If necessary, a scheduled office visit can be arranged.
12. Additional important dates:
    End of late registration: – **Friday, January 20, 2017**.
    Census date – **Wednesday, February 1, 2017**.
    Spring Break – **Monday, March 13, 2017** to **Friday, March 17, 2017**.
    Last day to drop classes – **Friday, March 31, 2017**.
    Summer and Fall 2016 registration begins – **Monday, April 3, 2017**.
    Last day of classes – **Friday, May 5, 2017**.

### Drop Policy:

Please refer to the University policy for dropping courses.

### Americans With Disabilities Act:

The University of Texas at Arlington is on record as being committed to both the spirit and letter of federal equal opportunity legislation; reference Public Law 92-112 - The Rehabilitation Act of 1973 as amended. With the passage of federal legislation entitled *Americans with Disabilities Act (ADA),* pursuant to section 504 of the Rehabilitation Act, there is renewed focus on providing this population with the same opportunities enjoyed by all citizens. As a faculty member, I am required by law to provide "reasonable accommodations" to students with disabilities, so as not to discriminate on the basis of that disability. Student responsibility primarily rests with informing faculty of their need for accommodation and in providing authorized documentation through designated administrative channels. Information regarding specific diagnostic criteria and policies for obtaining academic accommodations can be found at www.uta.edu/disability. Also, you may visit the Office for Students with Disabilities in room 102 of University Hall or call them at (817) 272-3364.

## Student Support Services Available:

The University of Texas at Arlington supports a variety of student success programs to help you connect with the University and achieve academic success. These programs include learning assistance, developmental education, advising and mentoring, admission and transition, and federally funded programs. Students requiring assistance academically, personally, or socially should contact the Office of Student Success Programs at 817-272-6107 for more information and appropriate referrals.

## Final Review Week:

A period of five class days prior to the first day of final examinations in the long sessions shall be designated as Final Review Week. The purpose of this week is to allow students sufficient time to prepare for final examinations. During this week, there shall be no scheduled activities such as required field trips or performances; and no instructor shall assign any themes, research problems or exercises of similar scope that have a completion date during or following this week unless specified in the class syllabi. During Final Review Week, an instructor shall not give any examinations constituting 10% or more of the final grade, except makeup tests and laboratory examinations. In addition, no instructor shall give any portion of the final examination during Final Review Week. Classes are held as scheduled during this week and lectures and presentations may be given.

## E-Culture Policy:

The University of Texas at Arlington has adopted the University email address as an official means of communication with students. Through the use of email, UT-Arlington is able to provide students with relevant and timely information, designed to facilitate student success. In particular, important information concerning registration, financial aid, payment of bills, and graduation may be sent to students through email. All students are assigned an email account and information about activating and using it is available at www.uta.edu/email. New students (first semester at UTA) are able to activate their email account 24 hours after registering for courses. There is no additional charge to students for using this account, and it remains active as long as a student is enrolled at UT-Arlington. Students are responsible for checking their email regularly.

## Ethics:

**Student Responsibility**

Undergraduate and graduate students assume full responsibility for knowledge of all University rules, regulations and deadlines published in the Undergraduate and Graduate Catalogs and of all departmental and program requirements concerning their degree programs.

**Academic Dishonesty**

All students are expected to pursue their academic careers with honesty and integrity. Academic dishonesty includes, but is not limited to, cheating on a test or other coursework, plagiarism (offering the work of another as one's own) and unauthorized collaboration with another person. Students found responsible for dishonesty in their academic pursuits are subject to penalties that may range from disciplinary probation, suspension or expulsion from the University. In accordance with the Rules and Regulations of the Board of Regents of The University of Texas System (Part One, Chapter VI), institutional procedures regarding allegations of academic dishonesty are outlined in Part Two, Chapter 2, of the U.T. Arlington Handbook of Operating Procedures. This information may be obtained by accessing the Dean of Students' Web site at www.uta.edu/studentaffairs/dos or the Student Judicial Affairs' Web site at www.uta.edu/studentaffairs/judicial affairs. Copies of each regulation can be obtained in the Dean of Students' Office on the lower level of the University Center.

**Definitions (UTA Handbook of Operating Procedures)**

F. scholastic dishonesty, including, but not limited to, cheating on an examination or an assignment, plagiarism, and collusion;

1. *cheating on an examination or an assignment* includes:
   a. copying the work of another, engaging in written, oral or any other means of communication with another, or giving aid to or seeking aid from another when not permitted by the instructor;
   b. using material during an examination or when completing an assignment that is not authorized by the person giving the examination or making the work assignment;
   c. taking or attempting to take an examination for another, or allowing another to take or attempt to take an examination for a student;

d. using, obtaining, or attempting to obtain by any means, the whole or any part of an un-administered examination or work assignment;
e. any act designed to give unfair advantage to a student or the attempt to commit such an act;

2. *plagiarism* means the unacknowledged incorporation of the work of another in work that is offered for credit;
3. *collusion* means the unauthorized collaboration with another in preparing work that is offered for credit.

The following is an excerpt from the College of Engineering's statement on Ethics, Professionalism, and Conduct of Engineering Students. Read the statement carefully, sign it, and return it to your instructor. You may make a copy for your records. Additional copies of this statement can be obtained from your instructor or the Office of the Dean of Engineering.

**STATEMENT ON ETHICS, PROFESSIONALISM, AND CONDUCT**
**FOR ENGINEERING STUDENTS**
COLLEGE OF ENGINEERING
THE UNIVERSITY OF TEXAS AT ARLINGTON

The College cannot and will not tolerate any form of academic dishonesty by its students. This includes, but is not limited to cheating on examination, plagiarism, or collusion.

**Cheating** on an examination includes:

1. Copying from another's paper, any means of communication with another during examination, giving aid to or receiving aid from another during examination;
2. Using any material during examination that is unauthorized by the proctor;
3. Taking or attempting to take an examination for another student or allowing another student to take or attempt to take an examination for oneself.
4. Using, obtaining, or attempting to obtain by any means the whole or any part of an un-administered examination.

**Plagiarism** is the unacknowledged incorporation of another's work into work which the student offers for credit.
**Collusion** is the unauthorized collaboration of another in preparing work that a student offers for credit.

I have read and I understand the above statement.

In addition, I understand that, in order to ensure fairness to all students, exams will be proctored and possibly videotaped.

Course and section number: ____EE 3444-001/101/102_____

Date: _____

Student's signature: _____

Student's name, printed: _____

Student's ID number: _____

Student's e-mail address: _____
(please print clearly)

Detach this page and return it to the instructor or GTA.